WHAT IS CLAIMED IS:

1. A translator tool for translating event-based test data containing intentionally injected timing irregularities to cycle-based test data without timing irregularities, comprising:

a normalization function that extracts said intentionally injected timing irregularities in said event-based test data and generates corresponding normalized event-based test data without said extracted timing irregularities; and

a cyclization engine that cyclizes said normalized event-based test data to generate corresponding cycle-based test data without said timing irregularities.

2. A translator tool in accordance with claim 1, wherein:

said normalization function compensates one or more data signals in said event-based test data file by any time difference between offsets of simulated device clock edges and respective expected offsets of said device clock edges.

3. A translator tool in accordance with claim 1, wherein:

said normalization function compensates one or more data signals in said event-based test data file by any time difference between offsets of simulated data signal edges and respective expected offsets of said data signal edges.

4. A translator tool in accordance with claim 1, comprising:

a memory for storing said extracted timing irregularities.

5. A translator tool in accordance with claim 4, wherein:

said stored extracted timing irregularities are formatted into a timing irregularities file readable by a cycle-based tester for reinjecting said extracted timing irregularities contained in said timing irregularities file into said cycle-based test data to test a device under test.

6. A translator tool in accordance with claim 1, wherein:

said timing irregularities comprise clock period jitter.

7. A translator tool in accordance with claim 1, wherein:

said timing irregularities comprise clock period drift.

8. A translator tool in accordance with claim 1, wherein:

said event-based test data with injected timing irregularities comprises a serial data signal simulated to test clock recovery circuitry of a device under test.

9. A method for translating event-based test data containing intentionally injected timing irregularities to cycle-based test data without timing irregularities, comprising:

detecting timing irregularities in said event-based test data;

extracting said detected timing irregularities from said event-based test data;

generating corresponding normalized event-based test data without said extracted timing irregularities; and

cyclizing said normalized event-based test data to generate corresponding cycle-based test data without said timing irregularities.

10. A method in accordance with claim 9, wherein:

said step for generating said corresponding normalized event-based test data without said extracted timing irregularities comprises compensating one or more data signals in said event-based test data file by any detected time difference between offsets of simulated device clock edges and respective expected offsets of said device clock edges.

11. A method in accordance with claim 9, wherein:

said step for generating said corresponding normalized event-based test data without said extracted timing irregularities comprises compensating one or more data signals in said event-based test data file by any time

difference between offsets of simulated data signal edges and respective expected offsets of said data signal edges.

12. A method in accordance with claim 9, comprising:

storing said extracted timing irregularities in a timing irregularities file readable by a cycle-based tester for allowing said cycle-based tester to reinject said extracted timing irregularities contained in said timing irregularities file into said cycle-based test data to test a device under test.

13. A method in accordance with claim 9, wherein:

said timing irregularities comprise clock period jitter.

14. A method in accordance with claim 9, wherein:

said timing irregularities comprise clock period drift.

15. A computer readable storage medium tangibly embodying program instructions implementing a method for translating event-based test data containing intentionally injected timing irregularities to cycle-based test data without timing irregularities, the method comprising the steps of:

detecting timing irregularities in said event-based test data;

extracting said detected timing irregularities from said event-based test data;

generating corresponding normalized event-based test data without said extracted timing irregularities; and

cyclizing said normalized event-based test data to generate corresponding cycle-based test data without said timing irregularities.

16. The computer readable storage medium of claim 15, wherein:

said step for generating said corresponding normalized event-based test data without said extracted timing irregularities comprises compensating one or more data signals in said event-based test data file by any detected time difference between offsets of simulated device clock edges and respective expected offsets of said device clock edges.

17. The computer readable storage medium of claim 15, wherein:

said step for generating said corresponding normalized event-based test data without said extracted timing irregularities comprises compensating one or more data signals in said event-based test data file by any time difference between offsets of simulated data signal edges and respective expected offsets of said data signal edges.

18. The computer readable storage medium of claim 15, the method further comprising the step of:

storing said extracted timing irregularities in a timing irregularities file readable by a cycle-based tester for allowing said cycle-based tester to reinject said extracted timing irregularities contained in said timing irregularities file into said cycle-based test data to test a device under test.

19. The computer readable storage medium of claim 15, wherein:

said timing irregularities comprise clock period jitter.

20. The computer readable storage medium of claim 15, wherein:

said timing irregularities comprise clock period drift.